REMARKS/ARGUMENTS

Claims 1-10 remain pending in this application. New claims 11 and 12 are added. Claims 8-10 are objected to for informalities. Claims 1-3 and 8-9 stand rejected under 35 U.S.C. 102(e) as being anticipated by Jones (US 6,310,909). Claims 1-3 and 8-10 stand rejected under 35 U.S.C. 102(e) as being anticipated by Long et al (5,991,311). Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art (AAPR) in view of Jones. Claims 6 and 7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art (AAPR) in view of Long et al.

Claims 1-10 are amended to more clearly define their respective languages. For example, claim 1 now recites, in part "A system for synchronizing voice signal received via a public switched telephone network (PSTN) and data signal received via a digital subscriber line; a PSTN interface coupled to transmit and receive the voice signal, a data DSL transceiver coupled to modulate and demodulate the data signal; a synchronization circuit coupled to synchronize said voice signal and said data signal..." Claims 2-10 are likewise amended. Claims 8-10 are further amended to overcome their respective objections.

Claims 4 and 5 are rewritten in independent form including all of the limitations of their respective base claims and any intervening claims and are thus believed to be allowable per Examiner's statements.

In view of the foregoing amendments and following remarks, reconsideration of the rejections of claims 1-3 and 6-10 is respectfully requested.

Claims Rejections under 35 U.S.C. §102(e)

Claims 1-3 and 8-9 stand rejected under 35 U.S.C. 102(e) as being anticipated by Jones (US 6,310,909). In rejecting claim 1 under 35 U.S.C. 102(e) as being anticipated by Jones, the Examiner asserts:

> Jones discloses a system for synchronizing a public switched telephone network (PSTN) clock and a digital subscriber line (DSL) clock, comprising:

> a PSTN interface (23) coupled to transmit and receive voiceband samples;
>
> a data DSL transceiver (as shown in Fig. 2) coupled to modulate (block 13) and demodulate (block 30) data to and from DSL samples;
>
> a synchronization circuit (block 29) coupled to synchronize said voiceband samples and said DSL samples; and
>
> a converter circuit (block 16 and 27) coupled to convert the synchronized voiceband samples and synchronized DSL samples between analog and digital formats

Applicants respectfully traverse this rejection. Fig. 2 of Jones discloses a DLS transceiver (4:46-50). Accordingly, interface 23 is used to transmit and receive DSL data. There is no disclosure in Jones, however, of transmitting voice signals over interface 23. Accordingly, Jones fails to teach or suggest "a PSTN interface coupled to transmit and receive the voice signal" as recited, in part, in claim1. Because Jones fails to handle voice signals, Jones also fails to teach or suggest "a synchronization circuit coupled to synchronize said voice signal and said data signal; and a converter circuit coupled to convert the synchronized voice signal and the synchronized data signal between analog and digital formats", as recited, in part, in claim1. Claim 1 is thus allowable over Jones for these additional reasons. Claim 1 and its dependent claims 2-3 are thus allowable over Jones for at least the reasons set forth above. Claims 8-9 are similarly allowable for at least the same reasons as is claim 1.

Claims 1-3 and 8-10 stand rejected under 35 U.S.C. 102(e) as being anticipated by Long et al. In rejecting claim 1 under 35 U.S.C. 102(e) as being anticipated by Long et al., the Examiner asserts:

> Long et al. disclose a system for synchronizing a public switched telephone network (PSTN) clock and a digital subscriber line (DSL) clock, comprising:
>
> a PSTN interface (tel line) coupled to transmit and receive voiceband samples;
>
> a data DSL transceiver (as shown in Fig. 11) coupled to modulate and demodulate data to and from DSL samples;

> a synchronization circuit (block 98) coupled to synchronize said voiceband samples and said DSL samples; and
>
> a converter circuit (block 44) coupled to convert the synchronized voiceband samples and the synchronized DSL samples between analog and digital formats

Applicants respectfully traverse this rejection. Long et al. disclose that "FIG. 11 is a diagram of a TCM-DSL modem". As is known to those skilled in the art and disclosed in Long et al., the telephone line (shown in Fig. 11 of Long et al. as TEL LINE) is used to transmit DSL data to and from the TCM-DSL modem shown in Fig. 11. Accordingly and as best understood, there is no disclosure in Long et al. of transmitting or receiving voice signals over the TEL LINE. Consequently, Long et al. fail to teach or suggest "a PSTN interface coupled to transmit and receive the voice signal" as recited, in part, in claim 1. Because the TCM-DSL modem shown in Fig. 11 of Long et al. fails to handle voice signals, Long et al. also fail to teach or suggest "a synchronization circuit coupled to synchronize said voice signal and said data signal; and a converter circuit coupled to convert the synchronized voice signal and the synchronized data signal between analog and digital formats", as recited, in part, in claim1. Claim 1 is thus allowable over Long et al. for these additional reasons.

Moreover, with respect to burst timing control 98, Long et al. discloses:

> "At the central office, burst timing control 98 receives clock 56 from the central office TCM ISDN burst-timing control circuit, or from extracting burst timing from an ISDN line signal. At the customer side, clock 56 is derived from the transmit burst received from the central office. ....When burst clock 56 is low, the transmit window is indicated, while the high phase of burst clock 56 indicates the receive window...."

In other words, as best understood, burst timing control 98 controls the timing for the transmit and the receive window of the data and, contrary to the Examiner's assertion, fails to disclose synchronization between voice signals and data signals. Claim 1 and its dependent

claims 2-3 are thus allowable over Long et al. for at least the reasons set forth above. Claims 8-10 are similarly allowable for at least the same reasons as is claim 1.

Claims Rejections under 35 U.S.C. §103

Claim 1 stands rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art (AAPR) in view of Jones. Claims 6 and 7 stand rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art (AAPR) in view of Long et al. In rejecting claim 1 under 35 U.S.C. 103, the Examiner asserts:

> AAPA discloses a system for synchronizing a public switched telephone network (PSTN) clock and a digital subscriber line (DSL) clock, comprising: (as shown in Fig. 1, prior art drawing)
>
> a PSTN interface (PSTN I/F) coupled to transmit and receive voiceband samples;
>
> a data DSL transceiver (ADLS ATU-C Transmitter and Receiver) coupled to modulate and demodulate data to and from DSL samples;
>
> a converter circuit (DAC) coupled to convert the synchronized voiceband samples and synchronized DSL samples between analog and digital formats
>
> AAPA disclose all the subject matter described above, except the specific teaching of a synchronization circuit.
>
> Jones, in the same filed of endeavor, teaches a timing recovery circuit (29 in Fig. 2) , which synchronization of two communicating transceivers (col6, L39-41).....

Applicants respectfully traverse this rejection. Jones is not concerned with and thus fails to disclose voice signals, as described above. Because Jones is silent on voice signals, Jones also fails to synchronize voice signals and DSL data signals. Moreover, as best understood and contrary to the Examiner's assertion, in Jones the timing recovery circuit is disclosed as synchronizing two communicating transceivers, and not to synchronize voice signals and DSL data signals:

"The analog to digital converter 27 may be synchronized to timing recovery circuit 29, which facilitates synchronization of two communicating transceivers.." (6:39-41).

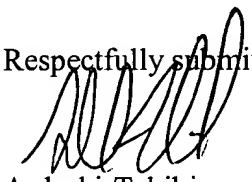
Claim 1 is thus allowable over applicant admitted prior art in view of Jones. Claims 6 and 7 stand rejected under 35 U.S.C. 103(as) as being unpatentable over Long et al. in view of Applicant admitted prior art (AAPR). Applicants respectfully traverse this rejection. Claims 6 and 7 are dependent on claim 1 and are thus allowable for at least the same reasons as is claim 1.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



ArdeshirTabibi
Reg. No. 48,750

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (650) 326-2422
Attachments
AT:deh
60195953 v1